IN THE CLAIMS

Please cancel claims 1-8.. All currently pending claims are reproduced in their entirety.

1-8. (Canceled)

9. (Previously Presented) A method for deterministic testing of edge-triggered logic, the method comprising:

setting a test signal in a test state so as to form a first scan chain that is responsive to a logic transition of a first clock signal and a second scan chain that is responsive to a logic transition of a second clock signal, the first and second scan chains each having an input for receiving scan data and an output for respectively providing the scan data; and

operating a third clock to control a latch interposed between the output of the first scan chain and the input of the second scan chain causing the latch to experience a hold state or a follow state, the hold state being experienced during a time period prior to the logic transition of the first clock signal and subsequent to the logic transition of the second clock signal such that data present at the output of the first scan chain prior to the logic transition of the first clock signal is held in the latch until after the logic transition of the second clock, the follow state being experienced outside the time period.